DSG-NPS R&D Meeting Minutes

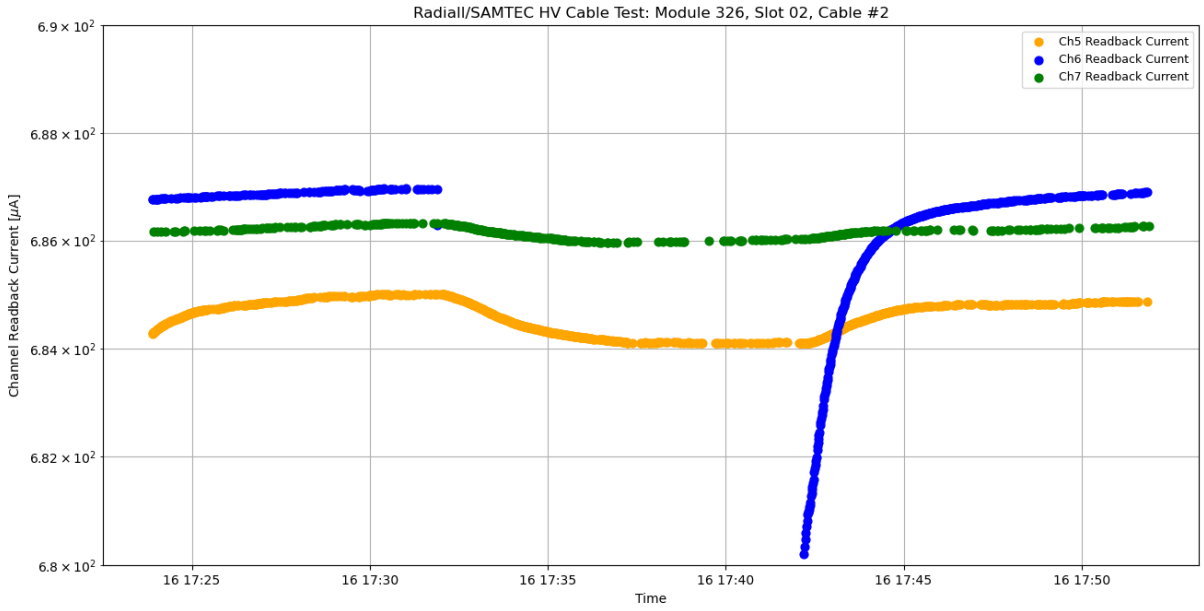
Date: April 27, 2021
Time: 11:00AM – 12:15 PM

Attendees: Peter Bonneau, Aaron Brown, Brian Eng, George Jacobs, Mindy Leffel, Marc McMullen, and Amrit Yegneswaran

1. HV supply cable testing

Peter Bonneau, Aaron Brown, Brian Eng, George Jacobs, Mindy Leffel, and Marc McMullen

1. Mindy Leffel has fabricated 15 of 40 HV supply cables
2. Reviewed plots for switching test completed for cable #2, channel #6
   - Zoomed in version of plot shows that current for adjacent channels was not steady while channel #6 was turned off
   - Current for channels #5 and #7 decreased by ~1 μA during the 10 minute period channel #6 was turned off
   - Will contact CAEN technical support to inquire as to why the current for channels #5 and #7 remained at this decreased level the entire time channel #6 was turned off



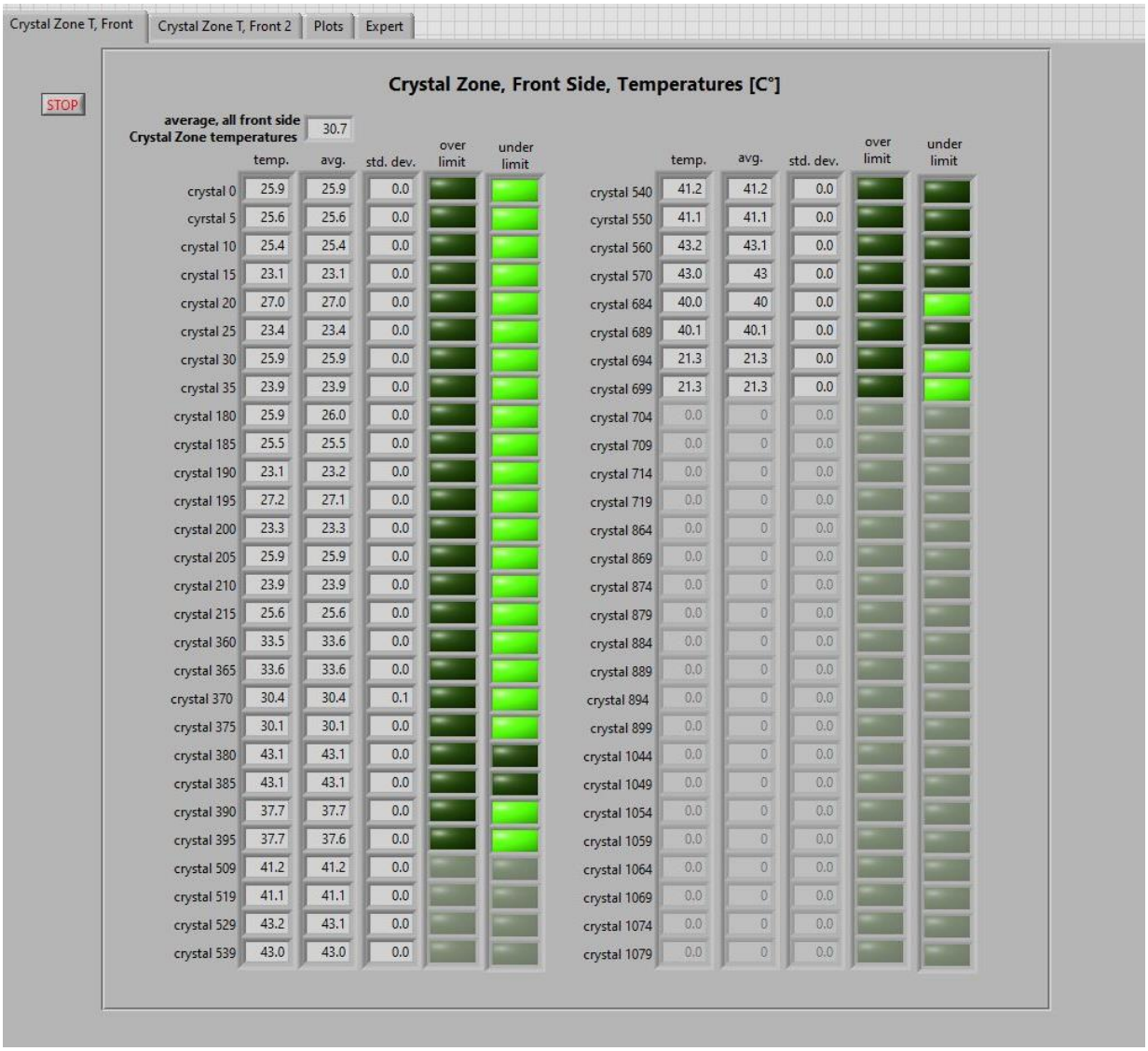
Plot of switching test for cable #2, channel #6 showing decrease in current for channels #5 and #7

3. Reviewed revised plot of no-load, long-term test of cable #1 in module #184
   - Plot will be revised to list all channel numbers for each band of current readback values
   - A long-term cable test will be done with load in the same module and a similar plot will be generated
4. Planning for a full density load test once 16 cables have been fabricated
   - Discussed fabrication of new load chassis to accommodate 16 cables; need to order additional SAMTEC board-mount connectors and resistors

2. Hardware interlock system development

Mary Ann Antonioli, Peter Bonneau, and Aaron Brown

1. Reviewed first draft of LabVIEW front panel for Crystal Zone temperatures
   - Will draw a directory tree to detail scope and number of tabs for each detector zone
   - Discussed design of matrix for temperature map of front and back of crystal zone; goal is to provide a color-coded temperature profile for each side of the crystal zone



Screenshot of front panel being designed to display crystal zone temperatures (front side shown)

2. Peter Bonneau and Aaron Brown will generate a timeline for all aspects of hardware interlock system development